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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,296	06/22/2001	David A. Fotland	20880-06029	9976

758 7590 07/06/2004

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EXAMINER	
HARKNESS, CHARLES A	
ART UNIT	**PAPER NUMBER**
2183	8

DATE MAILED: 07/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/888,296	Applicant(s) FOTLAND ET AL.	
	Examiner Charles A Harkness	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6, 7, and 8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Petition as received on 10/03/01; Declaration as received on 10/03/01; Information Disclosure Statement as received on 06/16/03; Information Disclosure Statement as received on 11/21/03; and Information Disclosure Statement as received on 03/29/04.

Specification

2. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Joy et al., U.S. Patent Number 6,542,991 (herein referred to as Joy).

4. Referring to claim 1 Joy has taught a multithreaded computer based system for enabling a command in a first thread to accessing data in a second thread comprising:

an embedded pipelined processor capable having a first program thread and a second program thread in an execution pipeline, said first program thread comprising a first set of instructions, said second program thread comprising a second set of instructions (Joy abstract,

figure 3, column 2 line 58-column 3 line 2, figure 8, column 8 lines 45-58), said embedded processor comprising:

a fetch unit for fetching an instruction from program memory (Joy figure 12 number 1216);

a decode unit for decoding said fetched instruction (Joy figure 12 number 1214);

an execution unit for executing said decoded instructions (Joy figure 12 numbers1232, 1234, 1236, 1238, 1240, 1242, 1244, 1246);

a write back unit for writing the results of said executed instruction to an identified storage location (Joy figure 12 number 1248 and 1250; the write ports);

a first set of data storage devices capable of storing a first state of said embedded processor (Joy figures 3 and 17A, column 8 lines 27-44; the register file or window of the thread contains the state, and the information and data of the thread), wherein said first state is the state of the embedded processor during the execution of the first program thread, including

a first control status register for identifying a first target set of data storage devices from which a first source operand of a first fetched instruction is to be retrieved from and for identifying a second target set of data storage devices to which a first result of a first executed instruction is stored (Joy figures 13 and 17A, column 27 lines 15-40; the window pointer points to the window where there are the "ins" of the function for a thread and the "outs") , wherein said first and second target set of data storage devices are different,

a second set of data storage devices capable of storing a second state of said embedded processor (Joy figures 3 and 17A, column 8 lines 27-44; the register file or window of the thread contains the state, and the information and data of the thread; figure 8 shows the cache being

shared by the two threads, but in different sections; each thread operates independently, and has its own individual data storage), wherein said second state is the state of the embedded processor during the execution of the second program thread, including:

a second control status register for identifying a third target set of data storage devices from which a second source operand of a second fetched instruction is to be retrieved from and for identifying a fourth target set of data storage devices to which a second result of a second executed instruction is stored (Joy figure 3, figures 5 and 8 column 3 lines 11-15, the storage cells are duplicated for the number of threads in the system, therefore for a 2 threaded system, there would be two window pointers; column 8 lines 27-44; the state of each thread, which would include its current window pointer, is saved so that when a context or thread switch is made, the window pointer is still valid), wherein said third and fourth target set of data storage devices are different;

a thread scheduler for identifying which of said program threads said embedded processor executes (Joy figure 6 column 16 line 42-column 17 line 32); and

an instruction set including an instruction that overwrites the first control status register when instructions associated with the first set of data storage devices are executed and overwrites the second control status register when instructions associated with the second set of data storage devices are executed (Joy column 8 lines 27-44column 29 lines 15-53; when a jump to subroutine or return call is made by the thread, the window pointer would be updated to point to the new window);

wherein said processor switches between said first and second state in a time period between the end of the execution of a first program instruction in the first thread and the

beginning of the execution of a second program instruction in the second thread (Joy column 8 lines 45-58; an instruction the first thread would finish executing, then the next instruction would cause a cache miss, and therefore a context switch, and then an instruction from the second thread would execute);

wherein said processor switches between said first and second states by changing a state selection register (Joy column 14 lines 5-16).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

Shaylor U.S. Patent Number 6,728,722 has taught a multi-threaded system with a general data structure for describing logical data spaces.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Patent Examiner

Art Unit 2183

June 21, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100